



AF 2184
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
Brian R. Bennett et al.)
Serial No.: 09/470,329)
Filed: December 22, 1999)
Title: PREVENTION OF LIVE-LOCK IN A MULTI-PROCESSOR SYSTEM
Assignee: Intel Corporation)
Examiner: Denise Tran
Group Art Unit: 2186
Docket: 884.174US1

APPEAL BRIEF UNDER 37 CFR § 41.37

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Sir:

The Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on February 22, 2005, from the Non-Final Rejection of claims 1-21 of the above-identified application, as set forth in the Non-Final Office Action mailed on November 16, 2004.

The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of 500.00 which represents the requisite fee set forth in 37 C.F.R. § 41.2(b)(2). The Appellants respectfully request consideration and reversal of the Examiner's rejections of the pending claims.



APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee,
INTEL CORPORATION.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

The present application was filed on December 22, 1999 with claims 1-21. A Non-Final Office Action was mailed October 24, 2002. A Final Office Action was mailed July 15, 2003. A Non-final Office Action (hereinafter "the Office Action") was mailed November 16, 2004. Claims 1-21 stand twice rejected, remain pending, and are the subject of the present Appeal.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent the filing of the response to the Non-Final Office Action dated October 24, 2002.

5. SUMMARY OF CLAIMED SUBJECT MATTER

Some aspects of the present inventive subject matter include, but are not limited methods, apparatus, and systems for the prevention of live-lock in a multi-processor system. Live-lock can occur, for example, when a first processor that is just reading a resource is always being granted the resource and a second processor that is trying to modify the resource is continually being retried. The Applicant's invention as claimed addresses the problem of live-lock, for example as in the embodiment shown in Figure 4a, by identifying a first bus transaction that attempts to *modify* a shared resource 404, and setting a status bit 408 indicating that a bus transaction attempting to modify the shared resource is pending. Each subsequent *nonmodifying* bus transaction for the shared resource is retried until the status bit is cleared at 412. (Page 4, lines 14-21)

In an embodiment, a method of the present invention in a microprocessor system, for example as shown in Figure 1, includes a processor 112 issuing a bus transaction that attempts to modify a cache line, (Page 6, lines 20-22) setting a status bit, for example status bit 306 of Figure 3, to indicate that a bus transaction attempting to modify the cache line is pending, and further including the steps of issuing a second bus transaction to read the cache line, retrying the second bus transaction if the status bit is set, reissuing the first bus transaction that attempts to modify the cache line; and granting the cache line for the reissued first bus transaction if the status bit is set for the cache line. (Page 8, line 19 through page 9, line 2).

Embodiments of the present invention include the microprocessor system 100 of Figure 1, including a plurality of processors 112a-h, (Page 4, lines 5-10) a resource shared by the plurality of processors, for example main memory 132, (Page 4, lines 24-26) and at least a system bus, for example buses 102, 104 and 106, interconnecting the shared resources with the plurality of processors. (Page 4, line 24 through page 5, line 4) An embodiment of microprocessor system 100 includes a plurality of data cache memories 114a-h. In an embodiment, the system includes at least two buses interconnecting the system memory with the plurality of data cache memories and the plurality of processors. (Page 4, line 24 through page 5, line 4)

Shared resources are not limited to main memory, but may include for example, I/O bridges. (Page 4, lines 16-23, and Figure 1) The microprocessor system may further include a system access controller 130, shown in detail in Figure 2, including a plurality of buffers 212, where each one of the plurality of buffers is associated with a bus transaction initiated on the at least one system bus by one of the processors. (Page 7, lines 14-19) As further shown in Figure 3, buffers 212 includes status indicators 302, 306, and 308, including a status indicator associated with each one of the plurality of buffers, the status indicator to indicate when a first one of the processors initiates a bus transaction attempting to modify the shared resource and the bus transaction is retried. (Page 7, line 30 through page 8, line 7)

In an embodiment of the invention, system access controller 130 is implemented as an integrated circuit. (Page 5, lines 15-17) The integrated circuit may include, as shown for example in Figure 3, a bus interface, for example 202a-b, 204a-b (Page 5, lines 21 through page 6, line 12) to control a plurality of bus transactions; a coherency module to maintain cache coherency for a plurality of cache lines, for example 206a-b (Page 6, lines 14-27) and a buffer manager 210 comprising a plurality of buffers 212, each one of the buffers to store information associated with one of the plurality of bus transactions received by the bus interface (Page 7, lines 8-12) and further, a plurality of status indicators 302, 306, and 308 as shown in Figure 3, to indicate that one of the bus transactions attempting to modify one of the cache lines is retried, at least one of the status indicators associated with each one of the buffers. (Page 7, line 20 through page 8, line 12)

Once a status bit has been set, various embodiments of the invention are used to clear the status bit. For example, clearing of the status bit occurs randomly. (Page 10, lines 1-2) In an embodiment, the status bit is cleared pseudo-randomly, or using a pseudo-random method. (Page 10, lines 4-5)

This summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and its legal equivalent for a complete statement of the invention.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-2, 4-5, and 7-8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Gilbert et al.* (U.S. 6,041,376) in view of *Arimilli et al.* (U.S. 6,138,218).

Claims 3, 6, and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Gilbert et al.* (U.S. 6,041,376) in view of *Arimilli et al.* (U.S. 6,138,218) as applied to claims 1 and 7 and further in view of *Donley et al.* (U.S. 5,761,446).

Claims 10-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Vogt et al.* (U.S. 5,897,656) in view of *Gilbert et al.* (6,041,376).

7. ARGUMENT

Applicable law

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.* The *Fine* court stated that:

Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so." *Id.* (emphasis in original).

Further,

The Office Action must provide specific, objective evidence of record for a finding of a teaching, suggestion, or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338 (Fed. Cir. 2002).

The M.P.E.P. adopts this line of reasoning, stating that:

In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

Rejection of claims 1-2, 4-5, and 7-8 (Gilbert et al./Arimilli et al.)

Claims 1-2, 4-5, and 7-8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gilbert *et al.* (U.S. 6,041,376) in view of Arimilli *et al.* (U.S. 6,138,218). Applicant traverses the rejection of claims 1-2, 4-5, and 7-8 because the Office Action fails to state a *prima facie* case of obviousness with respect to these claims for at least the reasons stated below.

Independent claim 1 recites, "setting a status bit to indicate that a bus transaction attempting to modify the shared resource is pending." Independent claim 7 recites, "setting a status bit to indicate that a bus transaction attempting to modify the cache line is pending." In an attempt to supply these elements, the Office Action on page 3 relies on Gilbert *et al.* Figure 8C, element 110, column 9, line 63-65, and column 11, lines 9-20. In Gilbert *et al.*, Figure 8C element 110 refers to "snoopy cache protocol engine sets hold flag and sets hold counter." At column 9, lines 63-65 Gilbert *et al.* states, "Field 82 stores the hold flag. When this flag is set, the snoopy cache protocol engine prevents other nodes or processors on the same node from accessing the data line." There is no teaching or suggestion in the cited portion of Gilbert *et al.* of setting a status bit to indicate an attempt to modify a shared resource.

The additional reference in Gilbert *et al.* mentioned in the Office Action, namely column 11, lines 9-20 states in part, "With the hold-for-forward-progress field 82 set, the snoopy cache protocol engine 32 can prevent access to all data requests from other nodes," and therefore only refers to what happens after the hold flag is set. Gilbert *et al.* does describe why the hold flag is set at column 2, lines 52-56 wherein, "In one aspect of the invention, a remote cache interconnect (also called a network controller) within a node has access to a hold flag. The remote cache interconnect sets or activates the hold flag when it receives data from the system interconnect for delivery to a requesting processor." Therefore, the hold flag referred to in the Office Action is used by Gilbert *et al.* to indicate that a remote cache has received data, and not to indicate "setting a status bit to indicate that a bus transaction attempting to modify the shared resource is pending," as recited in claim 1, or "setting a status bit to indicate that a bus transaction attempting to

modify the cache line is pending," as recited in claim 7. (emphasis added in both instances)

Further, the specification of the present application on page 7, line 21 through page 8, line 2 states,

In one embodiment, each one of the buffers contains an "in-use" bit 302, a memory address 304, and a set of status bits 306, 308. The in-use bit 302 indicates whether a particular buffer is available for use. The memory address 304 is the address identified by a particular bus transaction. The set of status bits 306, 308 indicate a variety of conditions, including but not limited to, the type of bus transaction. In one embodiment, one of the status bits 306 indicates that a transaction has been initiated that could potentially modify the resource. This status bit 306 is referred to herein as a "read-retry bit." The read-retry bit is set when the transaction that could potentially modify the resource is initiated. If the transaction completes successfully, the read-retry bit is cleared. If the transaction does not complete, for example if the transaction is retried, the read-retry bit remains set for that particular transaction. When the read-retry bit is set for a transaction, any nonmodifying transactions that attempt to use the same resource will be retried. (emphasis added)

Thus, the specification of the present invention clearly discloses bits used to indicate "in-use," and further discloses separate status bits used for a variety of conditions, including status bit 306, the read-retry bit, which is set when the transaction that could potentially modify the resource is initiated. These separate bits serve to indicate different conditions or events. The recitation in Gilbert *et al.* discloses the setting of the hold flag based on receiving data, which is a completely different reason than the basis used to determine if the status bit recited in claims 1 and 7 will be set. Therefore, it is clear that the "in use" hold flag of Gilbert *et al.*, which is used to indicate that a remote cache has received data, fails to teach or suggest the setting of a status bit to indicate that a bus transaction is attempting to modify either a shared resource or a cache line, as recited in claims 1 and 7 respectively in the present invention.

Further, Arimilli *et al.* at column 3, lines 5-12 states, "When a device snooping the system bus of a multiprocessor system detects an operation requesting data which is resident within a local memory in a coherency state requiring the data to be sourced from the device, the device attempts a intervention. If the intervention is impeded by a second

device asserting a retry, the device sets a flag to provide historical information regarding the failed intervention." (emphasis added) Therefore, Arimilli *et al.* discloses setting a bit as historical information regarding a failed intervention, and so fails to teach or suggest setting of a status bit to indicate that a bus transaction is attempting to modify either a shared resource or a cache line, as recited in claims 1 and 7 respectively in the present invention.

Because Gilbert *et al.* and Arimilli *et al.*, either alone or in combination, fail to teach or suggest "setting a status bit to indicate that a bus transaction attempting to modify the shared resource is pending," as recited in claim 1, and fail to teach or suggest "setting a status bit to indicate that a bus transaction attempting to modify the cache line is pending," as recited in claim 7, the cited documents fail to teach or suggest all the elements in claim 1 and all the elements in claim 7. Thus, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 1 and 7.

Claims 2 and 4-5 depend from claim 1, and therefore include all the elements of claim 1. Claim 8 depends from claim 7, and therefore includes all the elements of claim 7. For reasons analogous to those stated above and additional elements in the claims, Applicant respectfully submits that the Office Action fails to state a *prima facie* case of obviousness with respect to claims 2, 4-5, and 8.

In addition, the Office Action must provide specific, objective evidence of record for a finding of a teaching, suggestion, or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338 (Fed. Cir. 2002). The Office Action, in an attempt to meet this requirement, on page 20 states, "Evidence for the suggestion or motivation to combine comes from the references relied upon and the knowledge of one skilled in the art." However, the Office Action fails to point to anything of record in either Gilbert *et al.* or Arimilli *et al.* that would indicate a finding of a teaching, suggestion, or motivation to combine the references of Gilbert *et al.* and Arimilli *et al.* The Office Action on page 21 merely states,

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching

of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) (knowledge generally available to one of ordinary skill in the art) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

Applicant submits that these are mere statements of subjective belief. The Office Action has failed to point out in either Gilbert *et al.* or Arimilli *et al.*, for example, where maintaining the integrity of the flag is taught or suggested, or for example, where minimizing the storage requirements of the system is taught or suggested. Further, there is no indication in the Office Action of how maintaining the integrity of the flag and minimizing the storage requirements of the system would allow other traffic to proceed or to alleviate the prospect of live-lock. Hence, the statements in the Office Action are not supported by the record, and therefore fail to meet the standard of *In re Sang Su Lee*.

Thus, by failing to meet the standards of *In re Fine*, *In re Sang Su Lee*, and *M.P.E.P. § 2142*, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 1-2, 4-5, and 7-8. For at least the reasons stated above, Applicant requests withdrawal of the rejection and reconsideration and allowance of claims 1-2, 4-5, and 7-8.

Rejection of claims 3, 6, and 9 (Gilbert et al./Arimilli et al./Donley et al.)

Claims 3, 6, and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gilbert *et al.* (U.S. 6,041,376) in view of Arimilli *et al.* (U.S. 6,138,218) as applied to claims 1 and 7 above and further in view of Donley *et al.* (U.S. 5,761,446). Applicant traverses the rejection of claims 3, 6, and 9 because the Office Action fails to state a *prima facie* case of obviousness with respect to these claims for at least the reasons stated below.

In the present application, claim 3 recites, "clearing the status bit randomly," claim 6 recites, "clearing the status bit using a pseudo-random method," and claim 9 recites, "clearing the status bit pseudo-randomly." In contrast, Donley *et al.* at column 2, lines 50-58 recites,

Thus, an object hereof is to address "system livelock", especially with a "backoff" solution. A related object is to do so via "random backoff". Another related object to do so via a "stretch" mechanism, especially "random stretch". A further object is to implement such "random backoff" and/or "random stretch" mechanisms with addressing means which is adapted to generate the related random number (delay), especially where this is done with a linear feedback shift register, providing a "pseudo-random sequence"

Thus, Donley *et al.* is concerned with a random backoff which is described at column 1, lines 63-65 as a "mechanism which causes the AU to wait a 'random' time period t_b before rearbitrating for the system bus, then going direct to Resource request," and further, with a random stretch which is described at column 2, lines 1-4 as a "mechanism which enables the AU to immediately arbitrate for the system bus, and then, once access is granted, wait some 'random' time period t_s before attempting to use the resource." Donley *et al.* at column 3, lines 46-60, discloses generation of a random number. However, Donley *et al.* fails to teach or suggest clearing of a *status bit* randomly or pseudo-randomly as recited in claims 3, 6, and 9. The Office Action on page 7 admits that these elements are not shown in Gilbert *et al.* nor in Arimilli *et al.* Applicant agrees. Therefore, the combination of Gilbert *et al.*, Arimilli *et al.*, and Donley *et al.* fails to teach or suggest each of the elements as recited in claims 3, 6, and 9.

In addition, claims 3 and 6 depend from claim 1, and claim 9 depends from claim 7, and so claims 3, 6, and 9 include all the elements of the independent claim from which they depend. The Office Action's rejection of claims 3, 6, and 9 is based on Gilbert *et al.* and Arimilli *et al.* as applied to claims 1 and 7, and thus relies on Gilbert *et al.* and Arimilli *et al.* to supply all the elements included in claims 1 and 7. For reasons analogous to those stated above and additional elements in the claims, Applicant respectfully submits that neither Gilbert *et al.* nor Arimilli *et al.* nor Donley *et al.*, alone or in combination, teach or suggest all the elements of claims 3, 6, and 9. Thus, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 3, 6, and 9.

Further, on page 7 the Office Action states, "It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to apply the teaching of

Donley to the combine system of Gilbert and Arimilli because it would provide a random delay time, thereby optimizing live-lock avoidance and system performance as taught by Donley, col. 2, lines 61-63." Applicant disagrees. As noted above, *In re Fine*, *In re Sang Su Lee*, and *M.P.E.P.* § 2142 requires that in order to combine references, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings, and there must be a reasonable expectation of success. The Office Action fails to explain how providing a random delay time would optimize the systems proposed in Gilbert *et al.* and Arimilli *et al.* Further, there is no indication in the Office Action of whether there is a reasonable chance of success in combining the random delay time of Donley *et al.* with Gilbert *et al.* and Arimilli *et al.* Therefore, Applicant respectfully submits that the statements in the Office Action are conclusory statements of subjective belief. Thus, by failing to meet the standards of *In re Fine*, *In re Sang Su Lee*, and *M.P.E.P.* § 2142, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 3, 6, and 9.

For at least the reasons stated above, Applicant respectfully requests withdrawal of the rejection and reconsideration and allowance of claims 3, 6, and 9.

Rejection of claims 10-21 (Vogt *et al.*/Gilbert *et al.*)

Claims 10-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Vogt *et al.* (U.S. 5,897,656) in view of Gilbert *et al.* (6,041,376). Applicant traverses the rejection of claims 10-21 because the Office Action fails to state a *prima facie* case of obviousness with respect to these claims for at least the reasons stated below.

Claims 10 and 15 each recite, "a status indicator associated with each one of the plurality of buffers, the status indicator to indicate when a first one of the processors initiates a bus transaction attempting to modify the shared resource and the bus transaction is retried." Claim 17 recites, "a plurality of status indicators to indicate that one of the bus transactions attempting to modify one of the cache lines is retried, at least one of the status indicators associated with each one of the buffers." In an attempt to

supply these element, the Office Action relies on Vogt *et al.* at column 25, lines 61-64 and column 27, lines 32-45. Vogt *et al.* at column 27, lines 23-28 states,

In another aspect of the present invention as illustrated in FIG. 5B, the preferred buffer manager 210 contains a plurality of address comparators 510 which identify address conflicts. Typically, address conflicts arise when two different bus transactions relate to the same data value and occur at about the same time.

Further, Vogt *et al.* at column 27, lines 33-45 states,

When one the bus slaves 204 receives a bus transaction, the bus slave 204 forwards the address associated with the bus transaction to the address comparators 510 assigned to the same bus as the bus slave 204. The address comparators 510 compare the new memory address 504 with all of the memory addresses 504 existing in the in-use address cells 500. If the same memory address is detected in the in-use address cells 500, the address comparators 510 produce an output which notifies the bus slaves 204 that an address conflict exists. The bus slaves 204 then sends a retry signal to the processor 112 which initiated the bus transaction which created the address conflict. The processor 112 then initiates the bus transaction at a later date.

Thus, Vogt *et al.* is concerned with address conflicts, and status indicators that indicate address conflicts, not with "the status indicator to indicate when a first one of the processors initiates a bus transaction attempting to modify the shared resource" as recited in claims 10 and 15. Further Vogt *et al.* is not concerned with "status indicators to indicate that one of the bus transactions attempting to modify one of the cache lines" as recite in claim 17. The Office Action admits as much on page 8 with regards to claim 10, on page 10 with regards to claim 15, and on page 11 with regards to claim 17. In each of these instances, the Office Action relies on Gilbert *et al.* to supply these missing elements. For reasons analogous to those stated above with regards to claims 1 and 7, Applicant submits that Gilbert *et al.* also fails to recite the missing elements in claims 10, 15, and 22 as quoted above. Specifically, Gilbert *et al.* fails to teach or suggest "to indicate when a first one of the processors initiates a bus transaction attempting to modify the shared resource and the bus transaction is retried," and fails to teach or suggest "to indicate that one of the bus transactions attempting to modify one of the cache lines is retried."

Hence, neither Vogt *et al.* nor Gilbert *et al.*, either alone or in combination, teach or suggest all the elements of claims 10, 15, and 17. Thus, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 10, 15, and 17.

Claims 11-14, 16, and 18-21 depend from independent claims 10, 15, and 17 respectively, and therefore include all the elements of the independent claim from which they depend. For reasons analogous to those stated above and additional elements in the claims, Applicant respectfully submits that the Office Action fails to state a *prima facie* case of obviousness with respect to claims 11-14, 16, and 18-21.

Further, the Office Action on pages 10-11 states, "It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Gilbert with Vogt because it would provide guaranteed forward progress of the processor requests for data by preventing other processors from accessing data until the processor request is satisfied as taught by Gilbert col. 2, lines 41-50." Applicant disagrees and submits that the statement is merely a conclusory statement based on subjective belief, and further that the statement is not supported by the record.

As noted above, Gilbert *et al.* discloses setting a hold flag when it receives data from the system interconnect for delivery to a requesting processor, wherein when the hold flag is set, the snoopy cache protocol engine 32 can prevent access to all data requests from other nodes. In addition, Vogt *et al.* at column 27, lines 36-43 discloses, "The address comparators 510 compare the new memory address 504 with all of the memory addresses 504 existing in the in-use address cells 500. If the same memory address is detected in the in-use address cells 500, the address comparators 510 produce an output which notifies the bus slaves 204 that an address conflict exists. The bus slaves 204 then sends a retry signal to the processor 112 which initiated the bus transaction which created the address conflict." (emphasis added) Since Gilbert *et al.* makes no disclosure of checking for address conflicts, combining Gilbert *et al.* with Vogt *et al.* does not guarantee forward progress of processor requests, in that an address conflict can still exist that would prevent the bus transaction of Vogt *et al.* from occurring, despite any added elements from Gilbert *et al.*

Hence, the statements in the Office Action are not supported by the record, and further, fail to demonstrate that there is a reasonable expectation of success, and so fail to meet the standard of *In re Sang Su Lee* and *M.P.E.P.* § 2142. Thus, by failing to meet these standards, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 10-21.

For at least the reasons stated above, Applicant respectfully requests withdrawal of the rejection and reconsideration and allowance of claims 10-21.

Documents Cited but Not Relied upon for this Office Action

Applicant need not respond to the assertion of pertinence stated for the references cited but not relied upon by the Office Action since these references are not made part of the rejections in this Office Action. Applicant is expressly not admitting to this assertion and reserves the right to address the assertion should it form part of future rejections.

8. SUMMARY

For the reasons argued above, claims 1-2, 4-5, and 7-8 were not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Gilbert *et al.* (U.S. 6,041,376) in view of Arimilli *et al.* (U.S. 6,138,218).

In addition, for the reasons argued above claims 3, 6, and 9 were not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Gilbert *et al.* (U.S. 6,041,376) in view of Arimilli *et al.* (U.S. 6,138,218) as applied to claims 1 and 7 and further in view of Donley *et al.* (U.S. 5,761,446).

Further, for the reasons argued above claims 10-21 were not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Vogt *et al.* (U.S. 5,897,656) in view of Gilbert *et al.* (6,041,376).

It is respectfully submitted that the documents cited do not render claims 1-21 obvious, and that the claims are patentable over the cited documents. Reversal of the rejections and allowance of pending claims 1-21 is therefore respectfully requested.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Appeal Brief, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 22nd day of April, 2005.

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CLAIMS APPENDIX

1. (Previously Presented) A method of preventing live-lock in a multiprocessor system, the method comprising:
 - identifying a first bus transaction that attempts to modify a shared resource;
 - setting a status bit to indicate that a bus transaction attempting to modify the shared resource is pending; and
 - retrying each subsequent nonmodifying bus transaction for the shared resource until the status bit is cleared.
2. (Original) The method of claim 1 further comprising clearing the status bit when the first bus transaction completes.
3. (Original) The method of claim 1 further comprising clearing the status bit randomly.
4. (Original) The method of claim 1 further comprising clearing the status bit at periodic intervals.
5. (Original) The method of claim 4 wherein the periodical intervals are longer than a length of time for a bus transaction to complete.
6. (Original) The method of claim 1 further comprising clearing the status bit using a pseudo-random method.
7. (Original) A method of preventing live-lock in a multiprocessor system, the method comprising:
 - issuing a first bus transaction that attempts to modify a cache line;

setting a status bit to indicate that a bus transaction attempting to modify the cache line is pending;

issuing a second bus transaction to read the cache line;

retrying the second bus transaction if the status bit is set;

reissuing the first bus transaction that attempts to modify the cache line; and

granting the cache line for the reissued first bus transaction if the status bit is set for the cache line.

8. (Original) The method of claim 7 further comprising clearing the status bit when the reissued first bus transaction complete.

9. (Original) The method of claim 7 further comprising clearing the status bit pseudo-randomly.

10. (Previously Presented) A multiprocessor computer system comprising:

a plurality of processors;

a resource shared by the plurality of processors;

at least one system bus interconnecting the shared resource and the plurality of processors;

a plurality of buffers, each one of the plurality of buffers associated with a bus transaction initiated on the at least one system bus by one of the processors; and

a status indicator associated with each one of the plurality of buffers, the status indicator to indicate when a first one of the processors initiates a bus transaction attempting to modify the shared resource and the bus transaction is retried.

11. (Original) The multiprocessor computer system of claim 10 wherein four processors are coupled to each one of the system buses.

12. (Original) The multiprocessor computer system of claim 10 wherein the at least one system bus comprises two processor buses.

13. (Original) The multiprocessor computer system of claim 10 having four processors coupled to each one of the two processor buses.

14. (Original) The multiprocessor computer system of claim 13 further comprising an input/output bus.

15. (Previously Presented) A multiple bus, multiprocessor computer system comprising:

 a plurality of processors;
 a plurality of data cache memories;
 a system memory shared by the plurality of processors;
 at least two buses interconnecting the system memory with the plurality of data cache memories and the plurality of processors; and

 a controller comprising:
 a plurality of buffers, each one of the plurality of buffers associated with a bus transaction initiated on one of the buses by one of the processors; and
 a status indicator associated with each one of the plurality of buffers, the status indicator to indicate when a first one of the processors initiates a bus transaction attempting to modify the system memory and the bus transaction is retried.

16. (Original) The multiple bus, multiple processor system of claim 15 wherein each one of the at least two buses is coupled to four of the processors.

17. (Previously Presented) An integrated circuit comprising:

- a bus interface to control a plurality of bus transactions;
- a coherency module to maintain cache coherency for a plurality of cache lines;

and

- a buffer manager comprising,
 - a plurality of buffers, each one of the buffers to store information associated with one of the plurality of bus transactions received by the bus interface; and
 - a plurality of status indicators to indicate that one of the bus transactions attempting to modify one of the cache lines is retried, at least one of the status indicators associated with each one of the buffers.

18. (Original) The integrated circuit of claim 17 wherein the buffer manager further comprises logic to determine a type of bus transaction occurring on a bus.

19. (Original) The integrated circuit of claim 17 wherein the buffer manager further comprises logic to determine if two of the bus transactions are contending for a same cache line.

20. (Original) The integrated circuit of claim 17 further comprising logic to reset all of the plurality of status indicators.

21. (Original) The integrated circuit of claim 17 comprising 64 buffers and 64 status indicators.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Brian R. Bennett et al.

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